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Department of Electronics and Communication Engineering

M.Tech.-VLSI System Design (VSD)

Talk: 2

Report on Expert Talk

Date:20.01.2026

Speaker: Mr. Padmanabhan Kalyanaraman,

Software Enabling and Optimization Engineer, Altera

Title: FPGAs- Timing Analysis and Timing Closure using Quartus Prime Timing Analyzer

The expert talk on “FPGAs – Timing Analysis and Timing Closure using Quartus Prime Timing Analyzer” provided valuable insights into the importance of timing analysis in modern digital and FPGA-based designs. The **speaker of the talk highlighted several key concepts and industry practices**, emphasizing the role of timing analysis in achieving reliable and high-performance FPGA designs. The session emphasized the critical role of timing verification in ensuring reliable, high-performance semiconductor systems and highlighted current industry practices followed by design and verification engineers.

Importance of Timing Analysis

Timing analysis is a crucial step in digital design as it ensures that data signals propagate through the circuit within the required time limits defined by the clock. Even if a design is functionally correct, improper timing can lead to system failure.

Design Engineer vs Verification Engineer:

- **Design Engineering** is described as the *science of construction*, where engineers focus on developing architectures, writing RTL code, and implementing logic.
- **Verification Engineering** is referred to as the *art of breaking the design*, where engineers intentionally try to expose bugs and corner-case failures.

The speaker emphasized that there are **many job opportunities in verification engineering**, as the complexity of modern chips requires extensive validation before fabrication.

Verification in VLSI Design:

Verification involves generating comprehensive test cases to ensure the correctness of the design under all conditions. The following types of verification were discussed:

- **Functional Verification** – Front-end verification to ensure logical correctness
- **Formal Verification** – Mathematical proof-based verification
- **Physical Verification** – Layout-level checks
- **Timing Verification** – Back-end verification to ensure timing closure

Functional verification is primarily performed in the front-end stage, while timing verification is a critical back-end activity.

Reasons for Semiconductor Failures

Semiconductor designs may fail due to several reasons, including:

- Improper or bad timing constraints
- Functionally incorrect design
- Signal integrity issues

These failures highlight the importance of accurate timing analysis and constraint definition.

Factors Affecting Circuit Timing:

Several parameters influence the timing behaviour of a digital circuit:

- Length of interconnecting wires
- Resistance (R) and capacitance (C) of wires
- Operating temperature
- Supply voltage variations
- Logic depth of the timing path

Timing Analysis Techniques

Dynamic Timing Analysis (DTA)

Dynamic Timing Analysis evaluates both **functionality and timing** using switching activity and input test vectors. Although it provides realistic behavior, it has long runtimes and limited coverage depending on test vectors.

Static Timing Analysis (STA)

Static Timing Analysis focuses only on **timing verification** and does not require test vectors. It is significantly faster and provides full design coverage, making it the preferred industry approach.

Comparison between STA and DTA:

Feature	STA	DTA
Circuit view	Static	Dynamic (switching)
Runtime	Quick	Long
Coverage	Entire design	Vector-dependent
Checks	Timing only	Functionality and timing

Types of Timing Paths in FPGA Designs:

Common timing paths analyzed in FPGA designs include:

- Input to Register
- Register to Register
- Register to Output
- Input to Output

These paths are analyzed to identify critical paths that limit the maximum operating frequency.

Industry Verification Practices:

In real-world projects, engineers follow a **test plan or verification plan** that defines all required test cases, including corner and worst-case scenarios, to ensure robust design validation.

Launch and Capture Flip-Flops:

- The **launch flip-flop** initiates the data signal.
- The **capture flip-flop** receives the data.

The launch and capture clock edges generally differ by one clock cycle.

Timing Parameters:

- **Data Arrival Time (DAT):** Time taken for data to reach the destination register input
- **Clock Arrival Time (CAT):** Time taken for clock to reach the capture register
- **Data Required Time (DRT):** Time by which data must be stable

Setup and Hold Requirements:

- **Setup DRT:**
$$DRT(T_{\text{setup}}) = CAT - t_{\text{setup}} - \text{setup uncertainty}$$
- **Hold DRT:**
$$DRT(T_{\text{hold}}) = CAT + t_{\text{hold}} + \text{hold uncertainty}$$

Slack Analysis

Slack is the difference between required time and arrival time:

- **Positive Slack:** Timing requirements are met
- **Negative Slack:** Timing violation exists and optimization is required

Setup Slack Formula:

Setup Slack = Minimum Data Required Time – Maximum Data Arrival Time

Common Interview Questions Discussed:

- Why do standard cell libraries prefer D flip-flops?
- What are setup time and hold time, and what causes their violations?
- How do you identify the critical (longest) timing path in a circuit?

The expert talk provided a comprehensive overview of timing analysis and timing closure in FPGA designs. It highlighted the importance of static timing analysis, real-world industry practices, and key timing concepts required for reliable semiconductor design. Tools like **Quartus Prime Timing Analyzer** play a vital role in achieving timing closure and ensuring robust system performance.


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